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PATENT APPLICATION
Attorney's Docket No.: 1465 1003-004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Joshua H. Bretz, Abram P. Dancy, Leif E. LaWhite and Martin F. Schlecht		
Application No.:	09/611,383	Group:	2838
Filed:	July 7, 2000	Examiner:	Bao Q. Vu
Confirmation No.:	8478		
For:	Control of DC/DC Converters Having Synchronous Rectifiers		

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RESPONSE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Response is being filed in response to the Office Action mailed from the U.S. Patent and Trademark Office on March 28, 2003 in the above-identified application. Reconsideration and further examination are requested.

An extension of time to respond to the Office Action is respectfully requested. A Petition for Extension of Time and the appropriate fee are being filed concurrently with this Amendment.

Claims 1-8, 10-12, 56-59 and 77-84 were rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka (USP 5,939,871). Claim 13 was rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of Shinada (USP 5,708,571). It is noted that, although claim 9 was listed as being rejected at page 1 of the Office Action, there is no specific rejection of that

claim; however, it is assumed that the Examiner intended to apply the same rejection as to parallel claim 11. The rejections are respectfully traversed and reconsideration is requested.

The present invention was designed to control the amount of back drive current through a controlled rectifier transistor during operation of the transistor. To that end, as the current through a controlled rectifier approaches a minimum, which may be a negative minimum as illustrated in Fig. 22, an override control to the converter control circuit limits further reduction of the current. The current may be limited by increasing the output voltage using a constant current source characteristic 2205, a fold-forward characteristic 2204 or a fold-back characteristic 2206.

The Examiner has referred to elements 5 and 6 in Tanaka with respect to override control to effect the minimum current limit. It is submitted that Tanaka uses a diode rectifier D and not a controlled rectifier transistor, does not effect a minimum current limit, and in particular does not effect a minimum current limit at the output terminals as claimed.

As described in column 4 of Tanaka, lines 4-40, the comparators 3 and 4 which receive the reference potentials 5 and 6 monitor the current I_L through the inductor L. More specifically, the comparator 4 compares the current I_L to a lower current limit, minimum current I_{LB} during a light load mode.

Operation of the circuit during the light load mode is best illustrated in Figure 5A. When the output voltage on capacitor C drops below a set output voltage as determined by comparator 2 at time T_1, transistor 1 is turned on to cause a ramp up of current I_L. When current I_L reaches a peak current I_{LP} at time T_2, transistor 1 turns off and the current begins to ramp down. As a result, the output voltage V_{OUT} will reach a peak and also ramp down. When the inductor current I_L reaches a minimum value, in this case equal to zero, the control circuit 7 is enabled to watch the output voltage through comparator 2. When the output voltage drops below the set output voltage level at time T_4, transistor 1 again turns on and the cycle repeats.

Note that the inductor current is not controlled to the value I_{LB}. Rather, the current naturally falls after transistor 1 is turned off at T_2, and when it reaches the trigger level I_{LB}, the control circuit 7 is enabled to respond to the output voltage. Rather than limiting the inductor current to I_{LB}, Tanaka assures that the current has dropped to I_{LB} before allowing transistor 1 to turn on.

As can be seen from the above discussion, the Tanaka circuit does not rely on an override control to effect a minimum current limit through the inductor. In fact, minimum current would only be effected by the diode rectifier D, to zero, and not by an override control to a control circuit. By coincidence, Tanaka uses similar terms "minimum current" and "limit" for concepts which are unrelated to applicants step of effecting a minimum current limit.

Further, similar to Wilcox, *et al.*, which was discussed in the last response, Tanaka does not affect the output current from the output terminal V_{OUT} to a load. For example, if current were returned from the load into the capacitor C, the charging circuit described above would cease operation by failing to trigger comparator 2, but the circuit would not respond to limit the current received from the load at the output terminal. Depending on the load, the output current could go negative even though the minimum value of the inductor current is zero. By contrast, with the present invention as illustrated in Figure 22, the override control would drive the output voltage up to limit the current received from the load.

Tanaka does not attempt to control the output current, that is, the current through terminal V_{OUT}. Rather, the output current is completely dependent on the current drawn by a load. Thus, the circuitry of Tanaka does not "effect a minimum current limit of the output current" as recited in each of the independent claims.

In view of the above discussion, each of the independent claims 1, 56, 82, 83 and 84 should be allowed. Further, elements of dependent claims are not suggested by the cited references.

With respect to claims 3 and 58, there is no suggestion in Tanaka of increasing the voltage output. As can be seen in Figures 5A and 5B of Tanaka, the mean output voltage remains constant. There is a ripple, which would also be experienced in embodiments of the present invention, but the ripple is about a constant mean voltage. The only illustrated change in voltage (Fig. 6) is a reduction in output voltage which would result if the system remained in the light load mode of operation during heavy load.

With respect to claim 4, there is no suggestion in Tanaka of either a fold-back or fold-forward minimum current limit as illustrated in Fig. 22.

With respect to claims 9 and 11, there is no suggestion of an ORing transistor in Tanaka.

With respect to claims 12, 77, 82 and 83, there is no suggestion of setting the current limit I_{LB} negative; and as noted above, that current limit is not the minimum output current limit claimed.

With respect to claim 13, there is no suggestion of primary and secondary transformer windings in Tanaka.

With respect to claims 78 and 80, there is no suggestion of controlling voltage output to effect minimum current limit. Tanaka maintains a constant mean voltage.

With respect to claims 79 and 81, the current I_{LB} is effected by disabling the transistor 1.

In view of the above remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned at (978) 341-0036.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By _____
James M. Smith
Registration No. 28,043
Telephone: (978) 341-0036
Facsimile: (978) 341-0136

Concord, MA 01742-9133
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